A General Noise and S-Parameter Deembedding Procedure for On-Wafer High-Frequency Noise Measurements of MOSFETs

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Abstract—A general deembedding procedure using one "OPEN" and two "THRU" dummy structures for noise and scattering parameter deembedding based on cascade configurations is presented in this paper. This technique does not require any equivalent-circuit modeling of probe pads or interconnections. This deembedding procedure is valid for designs having interconnections with any kinds of geometries and for devices operated at frequencies of several tens of gigahertz.

Index Terms—High-frequency noise, noise deembedding, scattering parameters, S-parameter deembedding.

I. INTRODUCTION

With the continuous downscaling of device dimensions, the impact of the surrounding parasitics on a transistor characteristics has gained importance in the ac and noise measurements of a device-under-test (DUT), which includes a transistor, probe pads, and the metal interconnections between the probe pads and transistor. Since the probe pads and metal interconnections introduce additional parasitics, deembedding procedures for both measured scattering and noise parameters must be performed to get the intrinsic performance of a transistor. In the deembedding methods presented in [1]–[3], a parallel-series configuration assumes that the capacitive effect of interconnections is negligible and the inductive and resistive effects are dominant at the frequencies of interest. However, this might not be true for the designs with long interconnections or at operating frequencies at several tens of gigahertz. Therefore, the DUT has to be modeled as probe pads, interconnections, and a transistor connected in cascade configurations. The deembedding procedure presented in [4] is based on cascade configurations, but it still neglects the capacitive effect of the interconnections and requires specific equivalent-circuit models for both probe pads and interconnections, which makes the deembedding results rely on the accuracy of the equivalent-circuit models and the element values used in the calculation. This paper presents a general deembedding procedure based on the cascade configurations without the requirement of any equivalent-circuit models for the probe pads and interconnections.

II. THEORY OF NOISY TWO-PORT AND NOISE PARAMETER DEEMBEDDING

Deembedding techniques are based on the noise correlation matrix defined in [5] and [6]. In this method, the DUT is modeled in a cascade configuration, as shown in Fig. 1 and Y_{PAD} is the admittance between the signal pads and ground. Fig. 2 shows the layouts of a DUT and the dummy structures used in the proposed deembedding procedure. The "OPEN" dummy structure consists of RF probe pads without interconnections and the transistor. The "THRU1" dummy structure consists of the probe pads with the section of the interconnection (I_1) at the input port of the DUT and the "THRU2" dummy structure consists of the probe pads with the section of the interconnection (I_2) at the output port of

the DUT. Based on the nomenclature defined in Fig. 1 and the DUT and dummy structures shown in Fig. 2, the procedure for the noise and scattering parameter deembedding is listed as follows.

1) Measure the scattering parameters $[S^{\text{DUT}}]$, $[S^{\text{OPEN}}]$, $[S^{\text{THRU1}}]$ and $[S^{\text{THRU2}}]$ of the DUT, "OPEN," "THRU1," and "THRU2" dummy pads and convert $[S^{\text{OPEN}}]$ to $[Y^{\text{OPEN}}]$.
2) Measure the noise parameters—$NF_{\min}^{\text{DUT}}$, $Y_{\text{opt}}^{\text{DUT}}$ and R_n^{DUT} of the DUT and calculate the noise correlation matrix $[C_A^{\text{DUT}}]$, as defined in [5] and [6].
3) Calculate Y_{PAD} ($Y_{\text{PAD}} = Y_{11}^{\text{OPEN}} + Y_{12}^{\text{OPEN}}$) and the $[A^{\text{PAD}}]$ matrix of the probe pads, as defined in Fig. 1.
4) Calculate the $ABCD$ matrices $[A^{\text{THRU1}}]$ and $[A^{\text{THRU2}}]$ from $[S^{\text{THRU1}}]$ and $[S^{\text{THRU2}}]$.
5) Calculate $[A^{\text{IN}}]$ and $[A^{\text{OUT}}]$ by $[A^{\text{IN}}] = [A^{\text{THRU1}}][A^{\text{PAD}}]^{-1}$ and $[A^{\text{OUT}}] = [A^{\text{PAD}}]^{-1}[A^{\text{THRU2}}]$.
6) Convert $[S^{\text{DUT}}]$ to $[A^{\text{DUT}}]$ and calculate the $ABCD$ matrix $[A^{\text{TRANS}}]$ of the intrinsic transistor using $[A^{\text{TRANS}}] = [A^{\text{IN}}]^{-1}[A^{\text{DUT}}][A^{\text{OUT}}]^{-1}$.
7) Convert the $ABCD$ matrices $[A^{\text{IN}}]$ and $[A^{\text{OUT}}]$ to their Z matrices $[Z^{\text{IN}}]$ and $[Z^{\text{OUT}}]$.
8) Calculate the noise correlation matrix $[C_Z^{\text{IN}}]$ and $[C_Z^{\text{OUT}}]$ from $[Z^{\text{IN}}]$ and $[Z^{\text{OUT}}]$.
9) Convert the $[C_Z^{\text{IN}}]$ and $[C_Z^{\text{OUT}}]$ matrices to their chain matrix form ($[C_A^{\text{IN}}]$ and $[C_A^{\text{OUT}}]$).
10) Calculate the correlation matrix $[C_A]$ of the intrinsic transistor by $[C_A] = [A^{\text{IN}}]^{-1}([C_A^{\text{DUT}}] - [C_A^{\text{IN}}])([A^{\text{IN}}]^{\dagger})^{-1} - [A^{\text{TRANS}}][C_A^{\text{OUT}}][A^{\text{TRANS}}]^{\dagger}$.
11) Calculate the noise parameters—$NF_{\min}$, Z_{opt}, and R_n of the intrinsic transistor from $[C_A]$.

III. MEASUREMENTS AND DISCUSSIONS

Three different DUTs—PAD50×40M, INT160L, and INT160R and their corresponding dummy structures are designed for the verification of the algorithm. All test structures are designed as ground–signal–ground (GSG) configurations and fabricated in a standard 0.35-μm CMOS technology through the Canadian Microelectronics Corporation (CMC), Kingston, ON, Canada. In these structures, the dimension of probe pads is 50 μm × 40 μm and the channel length and width of the transistors are 0.35 μm and 12 ×10 μm, respectively. The dimensions of the metal interconnections I_1 and I_2 are approximately zero for PAD50×40M. For INT160L, I_1 is 160 μm × 1 μm and I_2 is ∼0 μm^2. On the other hand, for INT160R, I_1 is ∼0 μm^2 and I_2 is 160 μm ×1 μm. Using these fabricated structures, the scattering and noise parameters are measured by using the ATN NP5B S-Parameter and Noise Parameter Measurement System. Fig. 3 shows the measured Y_{11} versus frequency characteristics for three different "OPEN" structures—OPEN50×40M ($I_1 = I_2 \cong 0$ μm^2), OPEN160L ($I_1 = 160$ μm × 1 μm and $I_2 \cong 0$ μm^2), and OPEN160R ($I_1 \cong 0$ μm^2 and $I_2 = 160$ μm × 1 μm). It is shown that the metal interconnection introduces about 25% susceptance at 12 GHz and will be more at higher frequencies. Therefore, the distributed capacitive effect of interconnections is not negligible and the network of interconnections have to be modeled in cascade with the transistor instead of in series. Fig. 4 shows the measured (dashed lines with symbols) and deembedded (symbols) noise parameters versus frequency characteristics of PAD50×40M (circles), INT160L (triangles), and INT160R (squares) biased at $V_{\text{DS}} = 1.0$ V and $V_{\text{GS}} = 1.2$ V ($I_{\text{DS}} = 7.8$ mA) based on cascade configurations. It is shown that the metal interconnection (I_1) at the input port of a transistor has more impact on $\text{NF}_{\min}$ than that (I_2) at
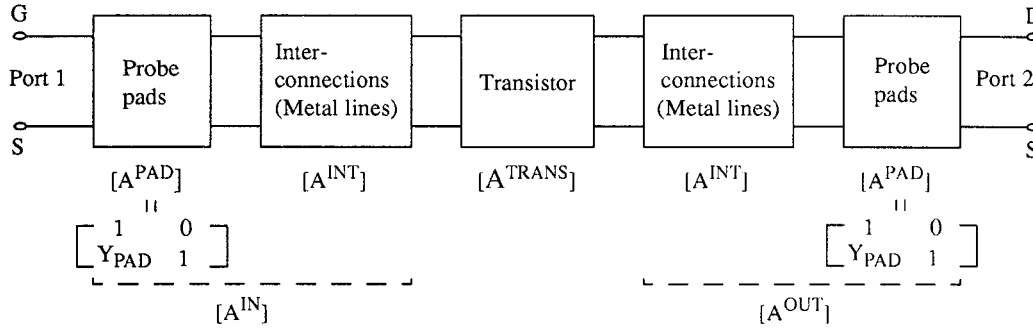
Fig. 1. Schematic diagram representing the structure of a DUT, which includes probe pads, metal interconnections, and a transistor modeled in cascade configurations.
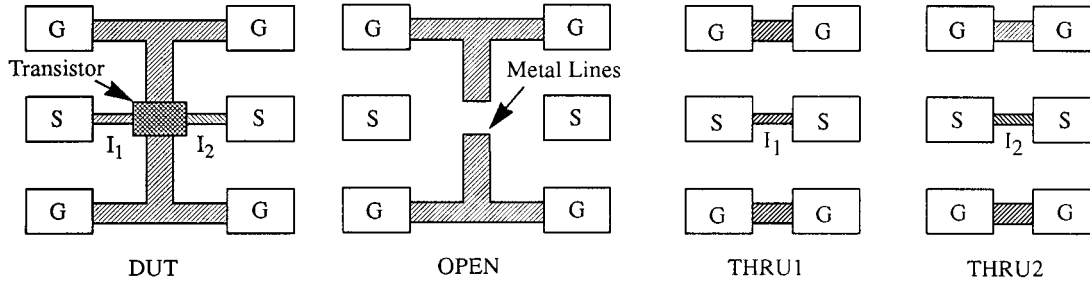

Fig. 2. DUT and its corresponding "OPEN," "THRU1," and "THRU2" dummy structures for the DUT used in the proposed deembedding procedure.
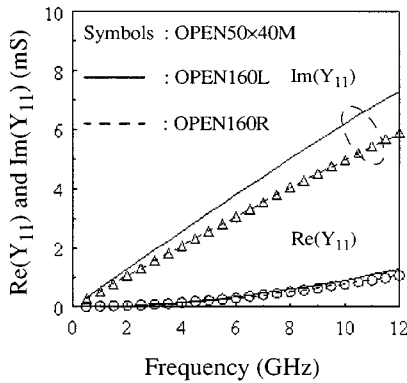

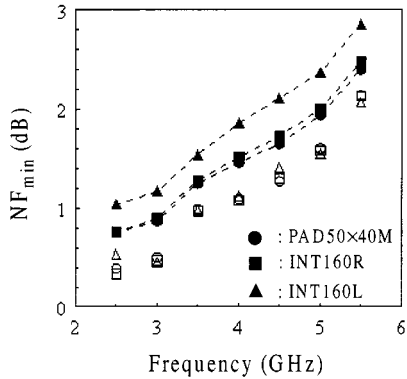Fig. 3. Measured Y_{11} versus frequency characteristics of different "OPEN" dummy structures.

Fig. 4. Extrinsic (dashed lines with symbols) and deembedded (symbols) minimum noise figure ($\mathrm{NF}_{\min}$) versus frequency characteristics of different test structures.

the output port because the resistive effect of the interconnection is amplified by the transistor to the output port.

IV. CONCLUSIONS

A general deembedding procedure of scattering and noise parameters based on cascade configurations for on-wafer RF measurements of MOSFETs has been presented in this paper and verified with measurements. This method improves the accuracy of deembedded results at high frequencies by taking the capacitive effect of metal interconnections into account.

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